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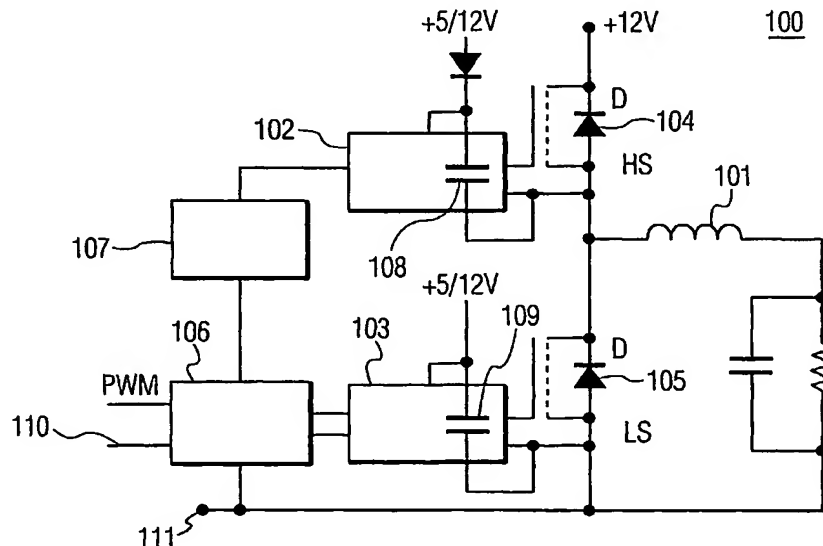
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[Continued on next page]

(54) Title: INTEGRATED INTERFACE CIRCUITRY FOR INTEGRATED VRM POWER FIELD EFFECT TRANSISTORS



(57) Abstract: A down converter includes an interface section, which connects the down converter to switches (104, 105) and respective driver circuits (102, 103), wherein the driver circuits and the switches are combined on an integrated circuit. The driver circuits include a high-side driver circuit (102), and a low-side driver circuit (103). The integration of the driver circuits with the switches reduces parasitic inductance, particularly in power applications.

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**Declarations under Rule 4.17:**

- *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii)) for the following designations AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VC, VN, YU, ZA, ZM, ZW, ARIPO patent (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ,*

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- *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii)) for all designations*

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